



PTO/SB/08A/B (09-08)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet	1	of	2	Attorney Docket Number	ASC-012DV
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Complete if Known

Application Number	10/788,741
Filing Date	February 27, 2004
First Named Inventor	Lee
Art Unit	2813
Examiner Name	Nguyen, Tuan H.

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Filing Date if Appropriate
		Number-Kind Code ² (if known)			
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Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	B30	0 829 908 A2 (EP)				

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	C75	"2-Bit/Cell EEPROM Cell Using Band-to-Band Tunneling for Data Read-Out," IBM Technical Disclosure Bulletin, Vol. 35, No. 4B (September 1992) pp. 136-140.	
	C76	Bouillon <i>et al.</i> , "Search for the optimal channel architecture for 0.18/0.12 μ m bulk CMOS Experimental study," IEEE, (1996) pp. 21.2.1-21.2.4.	

Examiner Signature	Date Considered
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				Art Unit	2813
				Examiner Name	Nguyen, Tuan H.
Sheet	2	of	2	Attorney Docket Number	ASC-012DV

C77	Grützmacher <i>et al.</i> , "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," <i>Applied Physics Letters</i> , Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.	
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C81	Maiti <i>et al.</i> , "Strained-Si heterostructure field effect transistors," <i>Semicond. Sci. Technol.</i> , Vol. 13 (1998) pp. 1225-1246.	
C82	Mizuno <i>et al.</i> , "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 5 (May 2000) pp. 230-232.	

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